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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,911	06/15/2001	John A. Michejda	MICHEJDA 4-6	9771

27964 7590 04/10/2003

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EXAMINER
FENTY, JESSE A

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/882,911	Applicant(s) MICHEJDA ET AL.	
	Examiner Jesse A. Fenty	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2, 4, 6, 7, 9, 10, 12, 14, 15, 21 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Liang et al. (U.S. Patent No. 6,346,729 B1).

In re claims 1 and 9, Liang discloses semiconductor device and method of making such device comprising:

A channel region (under gate oxide 3) located in a semiconductor substrate;

A trench (9, 12) located adjacent a side of the channel region;

An isolation structure (9) located in the trench;

A sidewall spacer (7) located over at least one sidewall of the trench distal the channel region;

and

A source/drain region (12) located over the isolation structure.

In re claims 2 and 10, Liang discloses the devices of claims 1 and 9 respectively, wherein the trench is a first trench and the semiconductor device further includes a second trench (9b, 12) located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure located in the first trench and the semiconductor device further includes a

second isolation structure (9b) located in the second trench, and wherein the source/drain region is a first source/drain region and the semiconductor devices further includes a second source/drain region (12) located over the second isolation structure.

In re claims 4 and 12, Liang discloses the devices of claims 1 and 9 respectively, wherein the source/drain region comprises silicon. The limitation, "epitaxial silicon" refers to a process for making the product. Applicant is reminded that, a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi* et al, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentablility of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. Therefore, the claim of "epitaxial" silicon, referring to the product of an epitaxial method of making, is not given patentable weight.

In re claims 6 and 14, Liang discloses the device of claim 1, wherein the sidewall spacer comprises a nitrided layer (column 3, lines 54-55).

In re claims 7 and 15, Liang discloses the devices of claims 1 and 9 respectively, wherein the isolation structure comprises an oxide.

In re claims 21 and 22, Liang discloses the devices of claims 1 and 9 respectively, wherein the sidewall spacer is not contiguous the side of the channel region.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liang as applied to claims 1 and 9 above, and further in view of Yu (U.S. Patent No. 6,287,925 B1).

In re claims 5 and 13, Liang discloses the devices of claims 1 and 9 respectively, but does not expressly disclose an oxide layer located between the sidewall spacer and the at least one sidewall of the trench. Yu discloses an oxide layer (218) disposed between a sidewall spacer (216) and a trench source/drain region (246). It would have been obvious for one skilled in the art at the time of the invention to insert an oxide layer as disclosed by Yu under the spacer layer of Liang for the purpose, for example, of creating a buffer layer between separate elements in the device (Yu; column 5, lines 22-24), thereby enhancing device performance.

4. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liang (as above).

In re claims 8 and 16, Liang discloses the devices of claims 1 and 9 respectively, wherein the source/drain region includes a lightly doped source/drain region (6b, 6c) having a dopant concentration in the range of 1E16 atoms/cm squared. Liang further discloses a high dopant concentration source/drain area (12) but does not expressly disclose the concentration to be up to about 1E22 atoms/cm squared. It would have been obvious to one having ordinary skill in the art

at the time the invention was made to dope the source/drain areas at a high level, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F. 2c 272, 205 USPQ 215 (CCPA 1980). Highly doping the source/drain regions decreases the resistance of the active region and enhances the speed of the device.

5. Claims 1, 3, 9, 11, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liang (as above) in view of Ishii et al. (U.S. Patent No. 5,086,322).

In re claims 1, 9 and 17, Liang discloses a semiconductor device, comprising:

A channel region (under gate oxide 3) located in a semiconductor substrate;

A trench (9, 12) located adjacent a side of the channel region;

An isolation structure (9) located in the trench;

A sidewall spacer (7) located over at least one sidewall of the trench distal the channel region; and

A source/drain region (12) located over the isolation structure.

Liang does not expressly disclose dielectric layers located over the semiconductor devices and having interconnect structures located therein. Ishii discloses dielectric layers (15, 16) overlying N and P- channel MISFET comprising interconnect structures (9). It would have been obvious for one skilled in the art at the time of the invention to cover the MIS device of Liang in the manner disclosed by Ishii for the purpose, for example, of providing device insulation and contact to the outside world.

In re claims 3 and 11, Liang in view of Ishii discloses the devices of claims 1 and 9 respectively, wherein the source/drain region (Ishii) comprises polysilicon.

In re claim 18, Liang in view of Ishii discloses the device of claim 17, wherein the trench is a first trench and the semiconductor device further includes a second trench (9b, 12) located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure located in the first trench and the semiconductor device further includes a second isolation structure (9b) located in the second trench, and wherein the source/drain region is a first source/drain region and the semiconductor devices further includes a second source/drain region (12) located over the second isolation structure.

In re claim 19, Liang in view of Ishii discloses the device of claim 17, wherein the isolation structure comprises an oxide.

In re claim 20, Liang in view of Ishii discloses the device of claim 17, wherein the semiconductor device is a PMOS, NMOS, or CMOS (Liang; column 2, lines 64-67).

Response to Arguments

6. Applicant's arguments with respect to claims 1-20 have been considered but are not persuasive

7. Applicant argues that device disclosed by Liang does not teach forming a sidewall spacer over at least one sidewall of the trench distal the channel region.

a. However, as appears in Figs. 7 and 8 of Liang, the disclosure appears to meet the limitation. The sidewalls (7) are directly over the sidewalls of the trench distal (away) from the channel region.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-746-3892 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A. Fenty
Examiner
Art Unit 2815

JAF
April 6, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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